Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.015”**

**G**

**G**

**S-D**

**S-D**

**F14**

**.015”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0035 x .0035”**

**Backside Potential:**

**Mask Ref: N0014L**

**APPROVED BY: DK DIE SIZE .015” X .015” DATE: 9/8/21**

**MFG: INTERFET THICKNESS .010” P/N: IF140ACFT**

**DG 10.1.2**

#### Rev B, 7/1